Technical Information

Admissible Power Dissipation

The indicated maximum admissible junction temperature must not be exceeded because this could damage or cause the destruction of the transistor crystal. Since the user cannot measure this temperature, data sheets also reveal the maximum admissible power dissipation P_{tot} usually in the form of a dreading curve (see diagram)

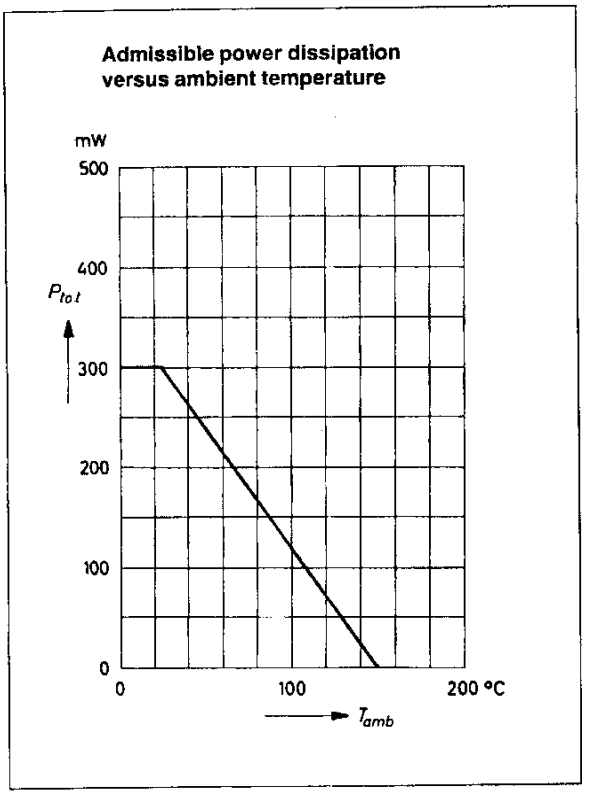
11 power dissipation is kept within these limits the maximum junction temperature will not be exceeded. This can easily be checked by using the equation

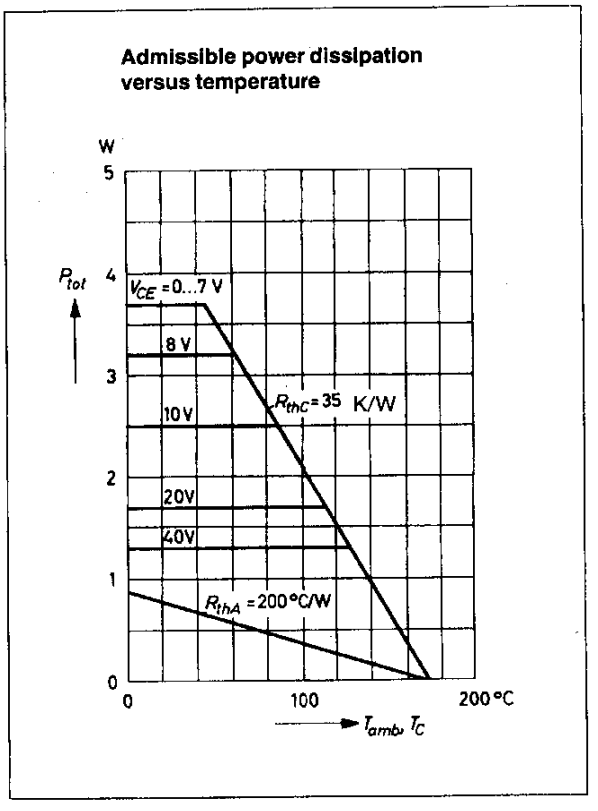
$T_j = T_{amb} + P_{tot} \times R_{th}$

For the thermal resistance R_{th} the junction to ambient thermal resistance R_{thA} is usually substituted in the case of small transistors (in the TO-18 or TO-92 package). In the case of power transistors (in the TO-202 or similar packages) which are usually mounted on a cooling fin or heat sink for the purpose of heat dissipation. the sum of lhe junction to case thermal resistance R_{thC} plus the heat sink to ambient thermal resistance P_{thS} plus - for more accurate calculations - the mounting surface to heat sink thermal resistance is substituted for the thermal resistance in this equation. In order to keep the mounting surface to heat sink thermal resistance low, a heat conducting compound (silicone grease) is 10 be applied to the mounting surface before the transistor is screwed on. If a mica insulation is used, the thermal resistance of the mica washer must be added which amounts to about 0 .5 K/W.

Directors for determining the thermal resistance R_{ths} for cooling fins can be 10und on page 6

Since the distribution of heat in the transistor crystal is not uniform and depends on voltage and current, some transistors are accompanied by dating curves showing P_{tot} as a function of T_C and T_{amb} with the collector voltage V_{CE} as parameter (see diagram below).





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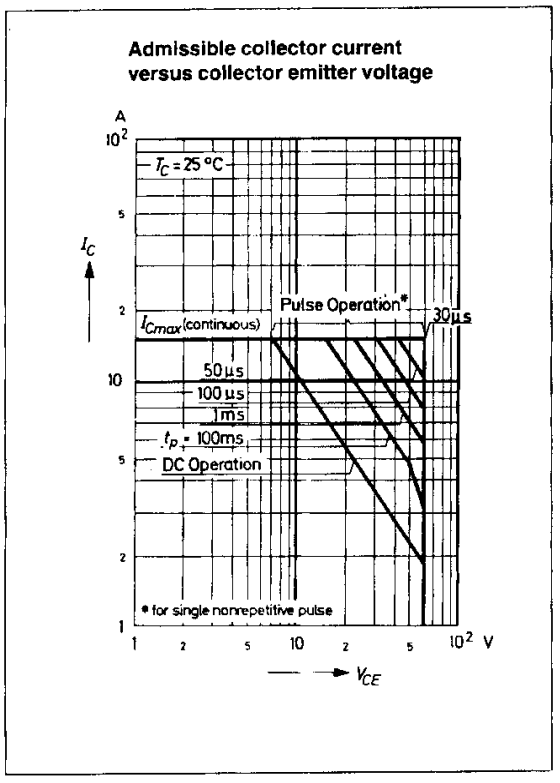

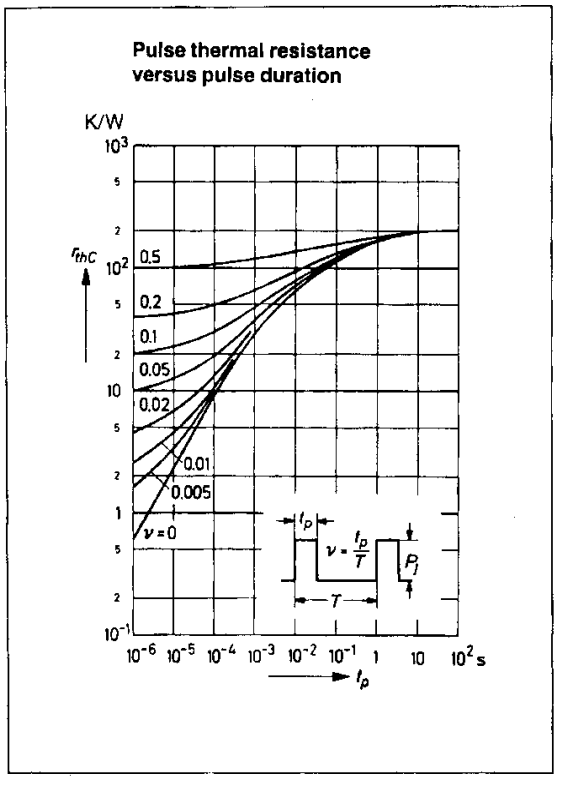

For some power transistors the data sheets also contain a diagram giving "admissible collector current" or "permissible operating range" which gives further information on admissible power dissipation. One example is illustrated in the diagram left

These diagrams are based on continuous power dissipation However, pulse power dissipation may usually exceed continuous power dissipation. To ascertain maximum admissible pulse power dissipation P_j, reference is made to the junction to ambient thermal resistance r_{thA} whose value can be derived from the $r_{th} = f(t_p)$ diagram below.

Use the equation

$$T_j = T_{amb} + P_I \cdot r_{thA}$$

Or, if the continuous power dissipation P_D is to be taken into consideration:

$$T_j = T_{amb} + P_D \cdot R_{thA} + P_I \cdot r_{thA}$$

If the transistor is mounted on a cooling 1in then the equation becomes:

$$Tj = T_{amb} + P_{tot} \cdot R_{thS} + RI \cdot r_{thC}$$

wherein P_{tot} is the mean value of pulse power dissipation p_j. Where continuous power dissipation must be considered in addition, the equation is expanded acrdingly

$$T_j = T_{amb} + P_{tot} \cdot R_{thS} + P_D \cdot R_{thC} + P_1 \cdot r_{thC}$$

wherein P_{tot} is the mean value of the total power dissipation.

The thermal resistance and pulse thermal resistance values derived from the data sheets apply without limitation only to small collector emitter voltages V_{CE}, between about 5 and 10V. For higher voltages these thermal resistance values have to be multiplied by a correction factor K_V which has to be calculated from the previously mentioned dating curves. The admissible power dissipation P_{totmax}, applicable to low collector voltages, must be divided by the admissible power dissipation $P_{tot\,V}$ for the higher collector voltage V

$$K_V = \frac{P_{tot\,max}}{P_{tot\,V}}$$

The complete equation for Tj then reads

$$Tj = Tamb + P_{tot} \cdot R_{thS} + P_D \cdot K_V \cdot R_{thc} + P_1 \cdot K_V \cdot r_{thC}$$